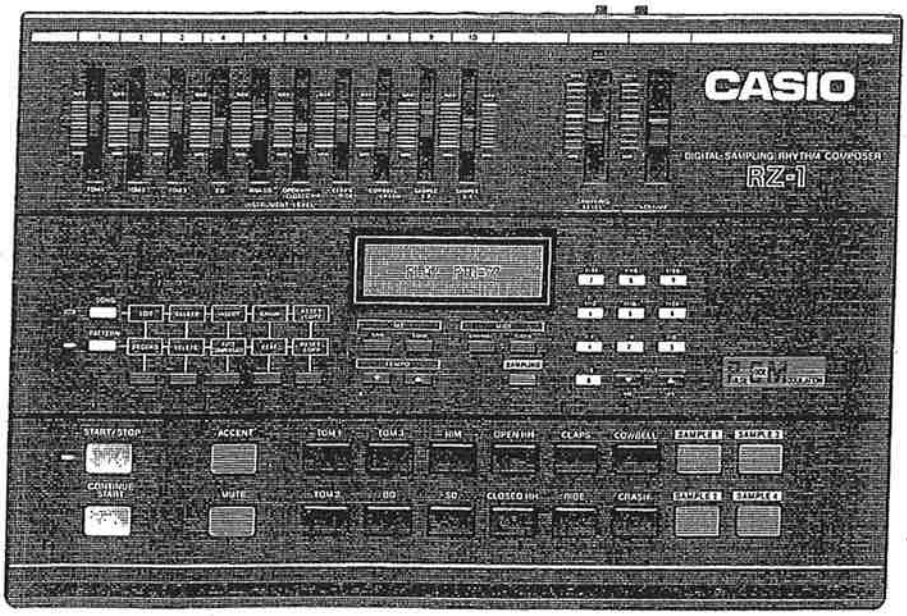
SERVICE MANUAL
& PARTS LIST (with price)

ELECTRONIC KEYBOARD

RZ-1

APR. 1986



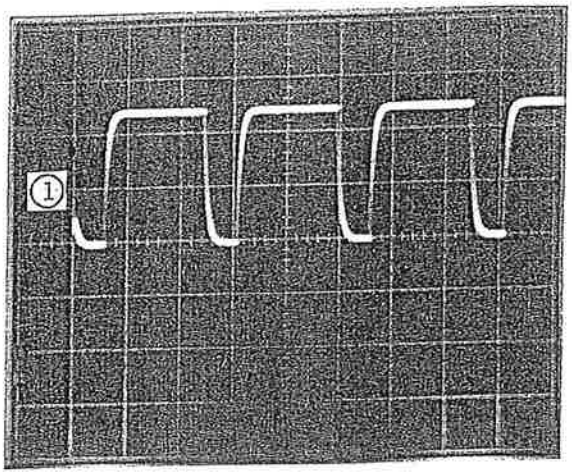
RZ-1

CASIO®

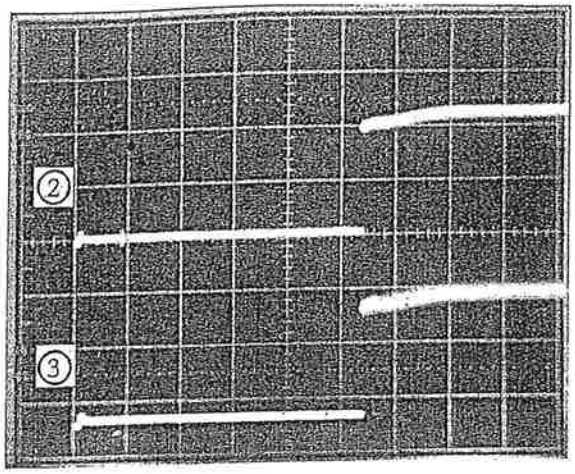
CONTENTS

5. MAJOR WAVEFORMS

Note: Prove 1:1

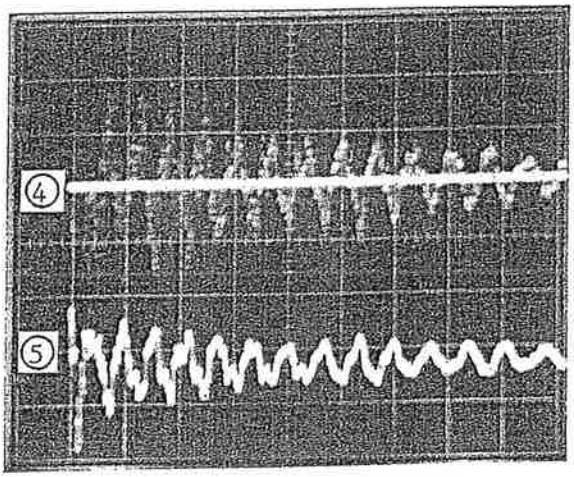


① TC4013 Clock pulse
PCB M0194-MA1M
TC4013 (1) Pin 3
2V/div, 5μs/div



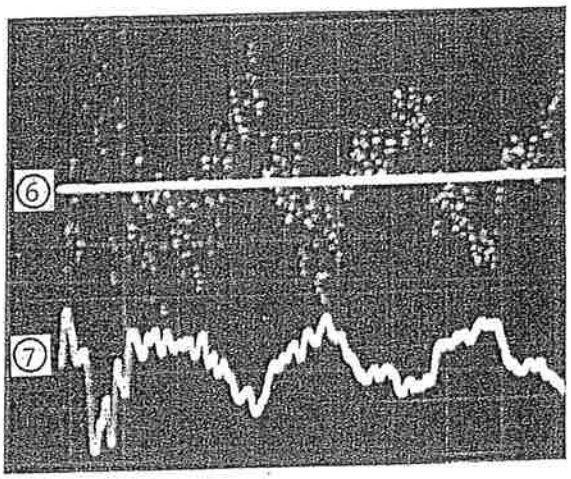
② μPD934G (B) Reset signal
PCB M0194-MA1M
SN74LS74AN Pin 6
2V/div, 0.2ms/div

③ μPD934G (C) Reset signal
PCB M0194-MA1M
SN74LS74AN Pin 8
2V/div, 0.2ms/div



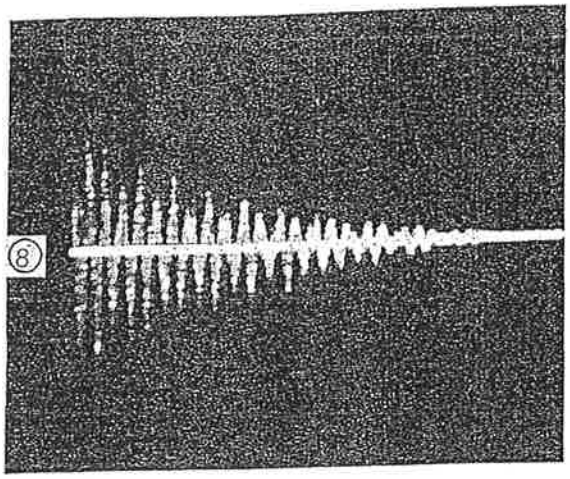
④ TOM1 Sound
PCB M0194-MA1M
FET 2SK163M Source
of B chip side
0.2V/div, 10ms/div

⑤ TOM1 Sound
PCB M0194-MA2M
LINE-OUT terminal
20mV/div, 10ms/div

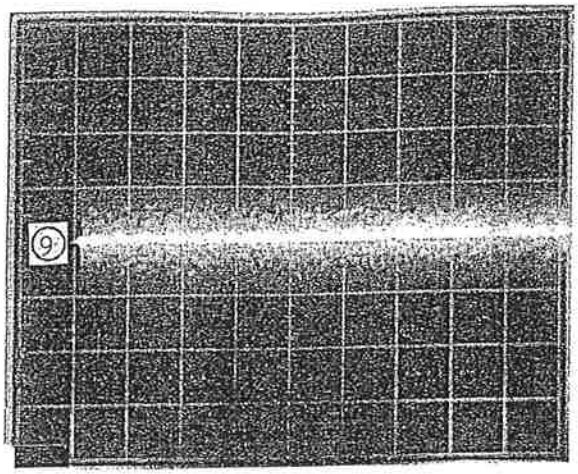


⑥ TOM1 Sound
PCB M0194-MA1M
FET 2SK163M Source
of B chip side
0.2V/div, 2ms/div

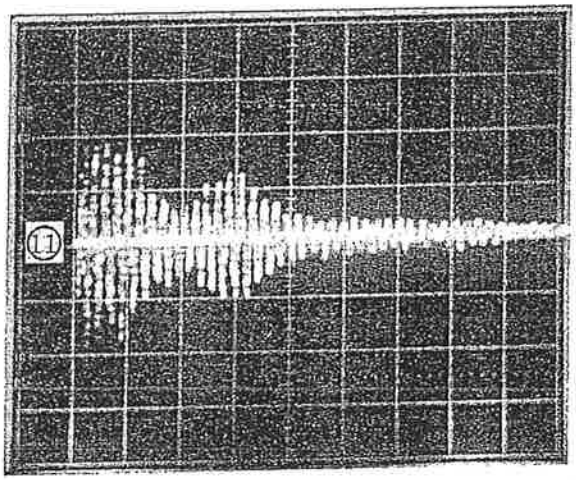
⑦ TOM1 Sound
PCB M0194-MA2M
LINE-OUT terminal
20mV/div, 2ms/div



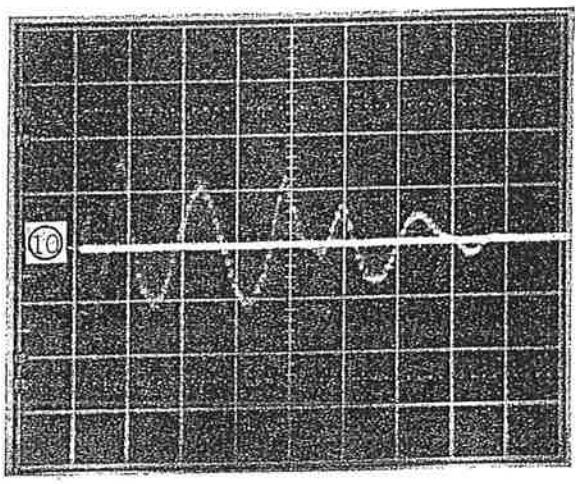
⑧ Snare Drum Sound
PCB M0194-MA1M
FET 2SK163M Source of B chip side
0.5V/div, 20ms/div



⑨ Crash Sound
PCB M0194-MA1M
FET 2SK163M Source of C chip side
0.5V/div, 10ms/div



⑩ Bass Drum Sound
PCB M0194-MA1M
FET 2SK163M Source of B chip side
0.5V/div, 10ms/div

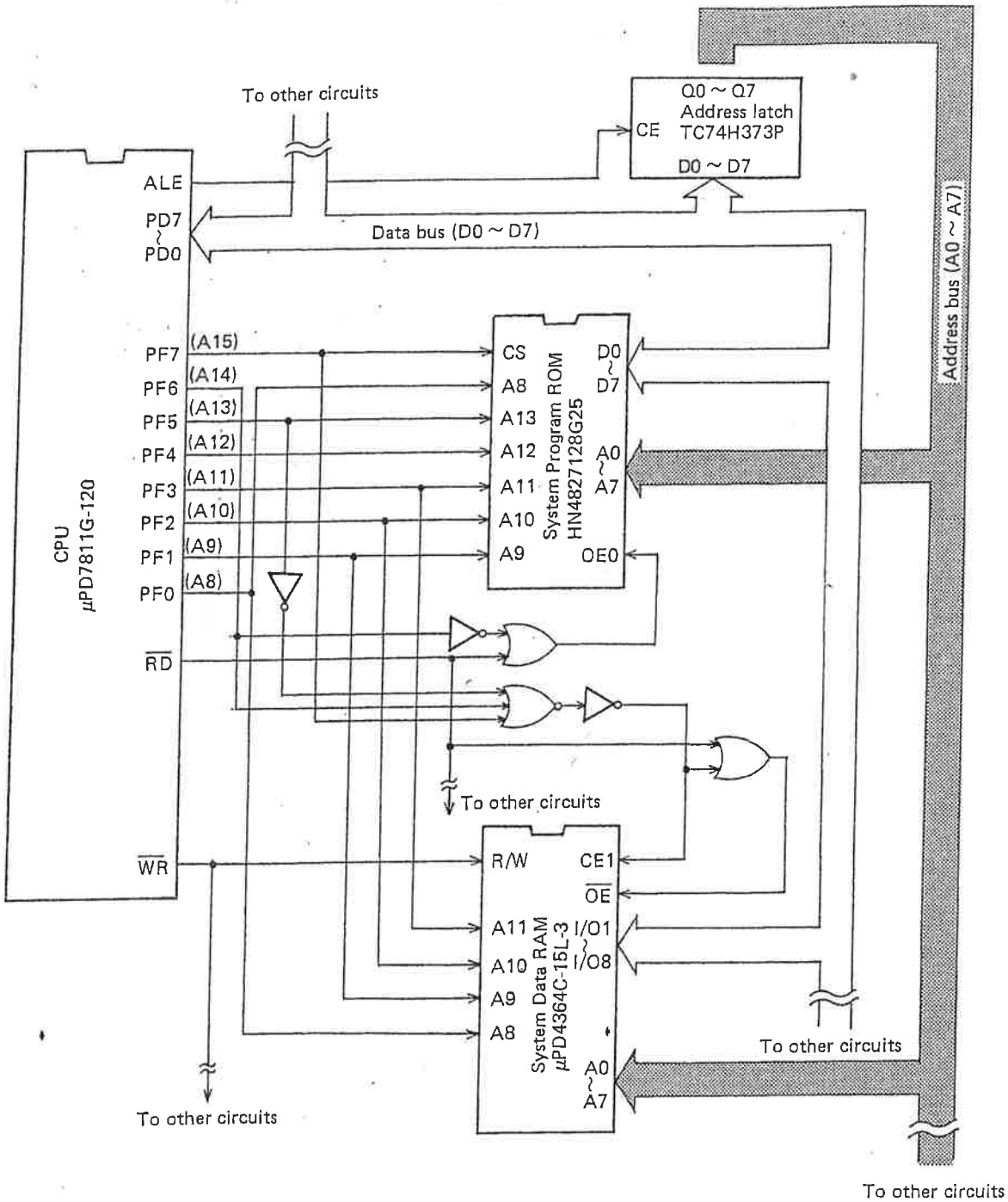


⑪ Cowbell Sound
PCB M0194-MA1M
FET 2SK163M Source of C chip side
0.5V/div, 10ms/div

6. CPU (μPD7811G-120) PIN FUNCTIONS

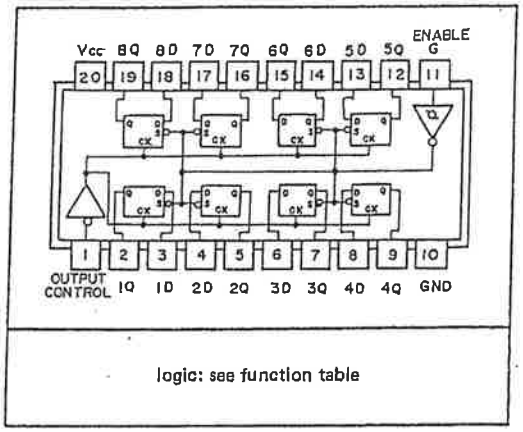
Pin No.	Terminal Name	IN/OUT	Functions
1~8	PA0 ~ 7	OUT	LCD control signals and key common signals
9	PB0	OUT	Change-over signal of TOM1 and TOM2 sound
10	PB1	OUT	Change-over signal of TOM3 and BD sound
11	PB2	OUT	Relay drive signal at "Power ON Mute" for Line-Out
12	PB3	OUT	Trigger signal of metronome
13	PB4	OUT	Percussion generator LSI (μPD934G(C)) reset signal. "L" active
14~16	PB5 ~ 7	OUT	LCD control signals
17	PC0	OUT	MIDI (Musical Instrument Digital Interface) data output
18	PC1	IN	MIDI data input
19	PC2	OUT	Control signal for percussion generator LSI (μPD934G(C))
20	PC3	IN	Data input from cassette tape
21	PC4	OUT	Change-over signal of address bus for sampling data RAM (μPD4364C-15L-1, 2)
22	PC5	OUT	Remote control (start/stop) signal for cassette tape recorder
23	PC6	OUT	Data output for cassette tape
24	PC7	IN	Foot-sustain input. "H": ON
28	$\overline{\text{RESET}}$	IN	Terminal stays "L" level for a while "At power ON" to initialize internal circuits.
30, 31	X2, X1	IN	12MHz clock pulse input
32	VSS		Ground (0V) source
33	AVSS		Ground (0V) source for internal DAC (Digital to Analog Converter)
34~41	AN0 ~ 7	IN	Sampling sound input
42	VREF		Reference voltage for internal DAC
43	AVCC		Reference voltage for internal DAC
44	$\overline{\text{RD}}$	OUT	Read signal output. Drops to "L" when CPU (μPD7811G) reads data from outer RAM (μPD4364C-15L-1, 2, 3)
45	$\overline{\text{WR}}$	OUT	Write signal output. Drops to "H" when CPU (μPD7811G) writes data into outer RAM (μPD4364C-15L-1, 2, 3)
46	ALE	OUT	Address latch enable signal output. Data bus (D0~D7) becomes address bus (A0 ~ A7) when "H".
47~54	PF0 ~ 7	OUT	Upper address bus (A8 ~ A15) for RAM (μPD4364C-15L-1, 2, 3)/ROM (HN4827128G25) and control signal for chip select circuits.
55~62	PD0 ~ 7	IN/OUT	Data bus (D0 ~ D7)
63	VDD		+5V source
64	VCC		+5V source

7. SYSTEM PROGRAM ROM & SYSTEM DATA RAM ACCESSES



64 Kbit of System data RAM is the data area for system execution. System Program ROM has 128Kbit capacity and contains the program for system execution.
The lower address signals (A0 ~ A7) are provided from data bus (D0 ~ D7). When signal ALE of CPU is "H", data signals (D0 ~ D7) are set in the Address latch and become the lower address bus.
The upper address signals (A8 ~ A12) are provided directly from the CPU.

SN74LS373, SN74S373 . . . J OR N PACKAGE
(TOP VIEW)

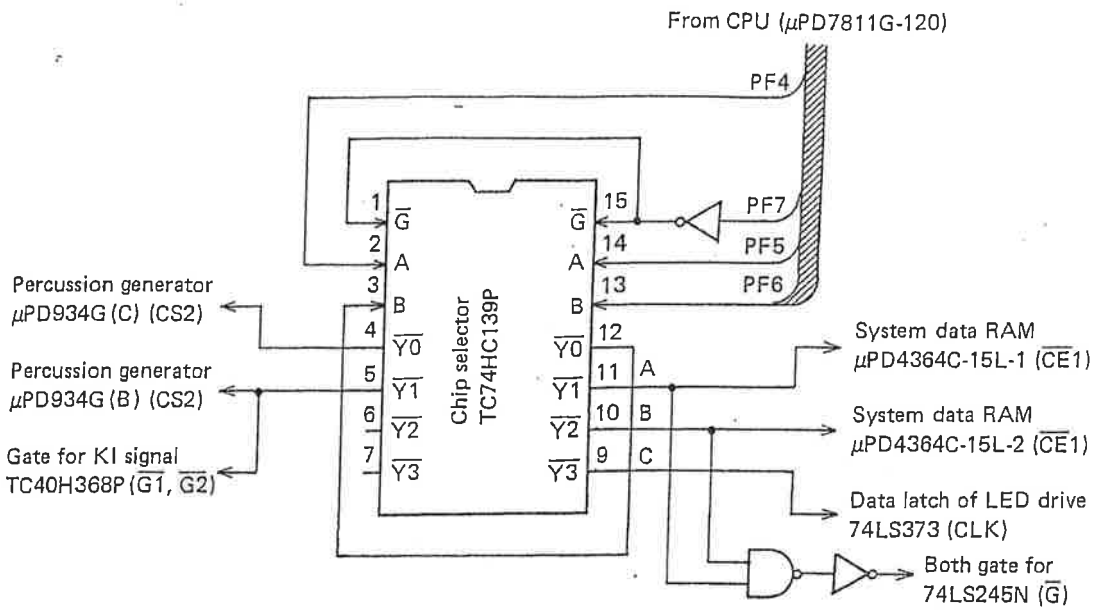


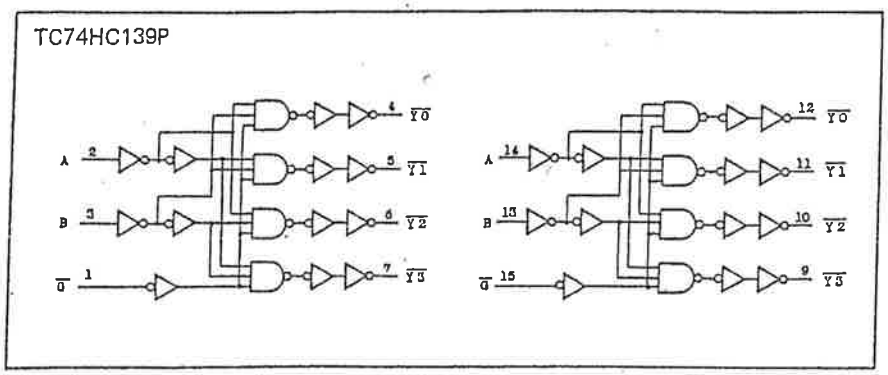
'LS373, 'S373
FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

8. CHIP SELECTOR

Chip selector (TC74HC139P) outputs the following signal.





FUNCTION TABLE

INPUTS			OUTPUTS				SELECTED OUTPUT
ENABLE	SELECT						
$\overline{G}$	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	
H	*	*	H	H	H	H	NONE
L	L	L	L	H	H	H	$\overline{Y0}$
L	L	H	H	L	H	H	$\overline{Y1}$
L	H	L	H	H	L	H	$\overline{Y2}$
L	H	H	H	H	H	L	$\overline{Y3}$

Note
* : Either

9. PERCUSSION GENERATOR (μPD934G) PIN FUNCTIONS

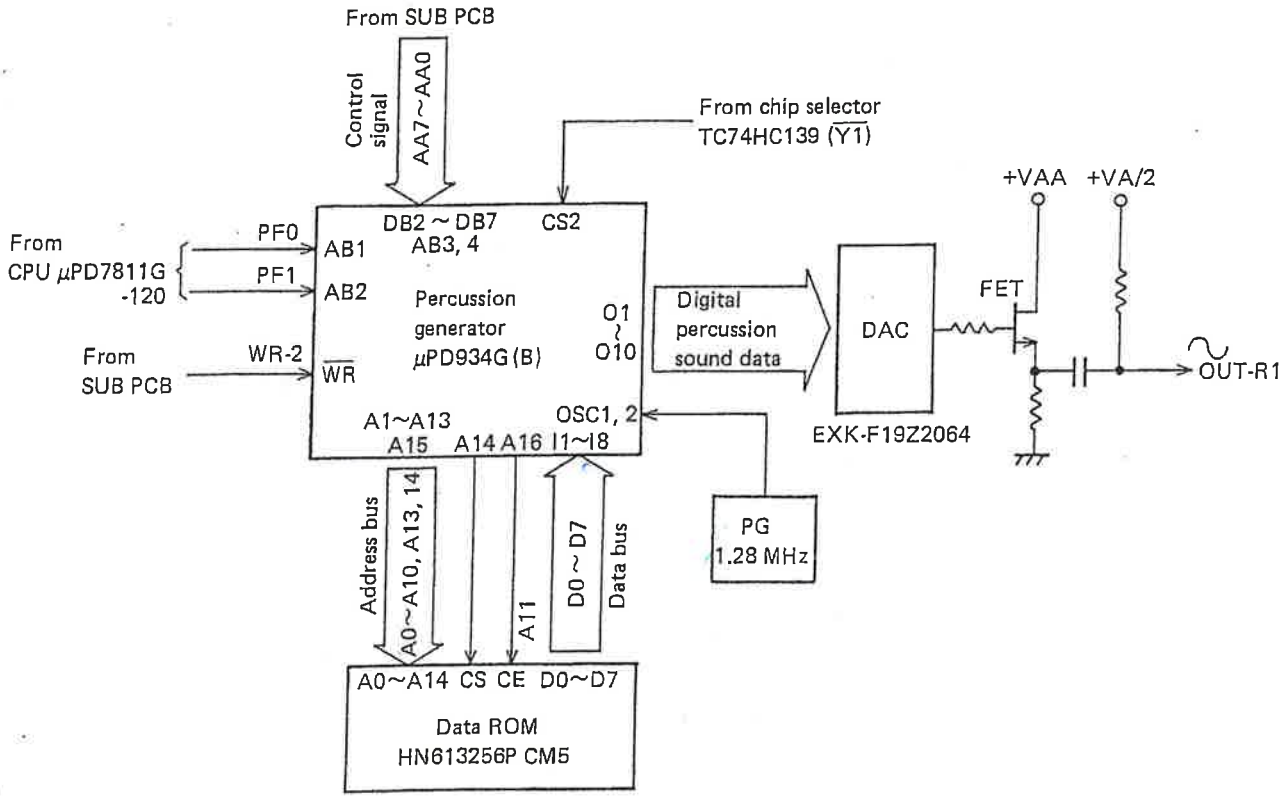
Note: B chip: μPD934G (B), C chip: μPD934G (C)

Pin No.	Terminal Name	IN/OUT	Chip	Functions
6 ~ 15	O10 ~ 1	OUT	B	Digital signal for percussion sound output
			C	Digital signal for percussion and sampling sound output
16, 17	AB3, 4	IN	B	Waveform control signal for percussion sound
			C	Waveform control signal for percussion and sampling sound
18~21	DB2~5	IN	B, C	4-bit data bus inputs from CPU (μPD7811G-120)
22, 23	DB6, 7	IN	B	Volume control signal for percussion sound
			C	Volume control signal for percussion and sampling sound
25	CLOCK	OUT	B	80KHz clock pulse output (for 1.28MHz clock pulse input)
			C	80KHz clock pulse output (for 1.333MHz clock pulse input)
26	GND		B, C	Ground (0V) source
27	VDD		B, C	+5V source
28	T1	IN	C	Control signal for percussion generator (μPD934G (C))
29, 30	OSC1, 2	IN	B	1.28MHz clock pulse input
			C	1.333MHz clock pulse input
32	RES	IN	B, C	Reset pulse input ("L" active). LSI's internal circuits are set at initial position when power is switch on.
33, 34	AB1, 2	IN	B, C	Control signal of internal address RAM
35, 36	CS1, $\overline{CS2}$	IN	B, C	Chip select signal input. CS1: "H" level fix, CS2 depends on signal from Decoder (TC74HC139).
37	$\overline{WR}$	IN	B	Write signal input. LSI receives data from data ROM (HN-613256P CM5) when drops to "L" level.
			C	Write signal input. LSI receives data from data ROM (HN-613256P CM6) or sampling RAMs (μPD4364C-15L-1, 2) when drops to "L" level.
39~46	I8 ~ 1	IN	B	8-bit data bus (D7 ~ D0) inputs from data ROM (HN613256P-CM5)
			C	8-bit data bus (DD7 ~ DD0) inputs from data ROM (HN613256P-CM6) or sampling RAMs (μPD4364C-15L-1, 2)
47~57 59~62	A1~A15	OUT	B	Address bus (A0 ~ A14) for data ROM (HN613256P-CM5)
			C	Address bus (A0 ~ A14) for data ROM (HN613256P-CM6) or sampling RAMs (μPD4364C-15L-1, 2)

Pin No.	Terminal Name	IN/OUT	Chip	Functions
58	GND		B, C	Ground (0V) souce
63	A16	OUT	B, C	Chip select signal for data ROM (HN613256P-CM5, 6)
64	A17	OUT	C	Chip select signal for sampling RAMs (μPD4364C-15L-1, 2)

10. PERCUSSION GENERATOR CIRCUIT

10-1. μPD934G (B chip) Block

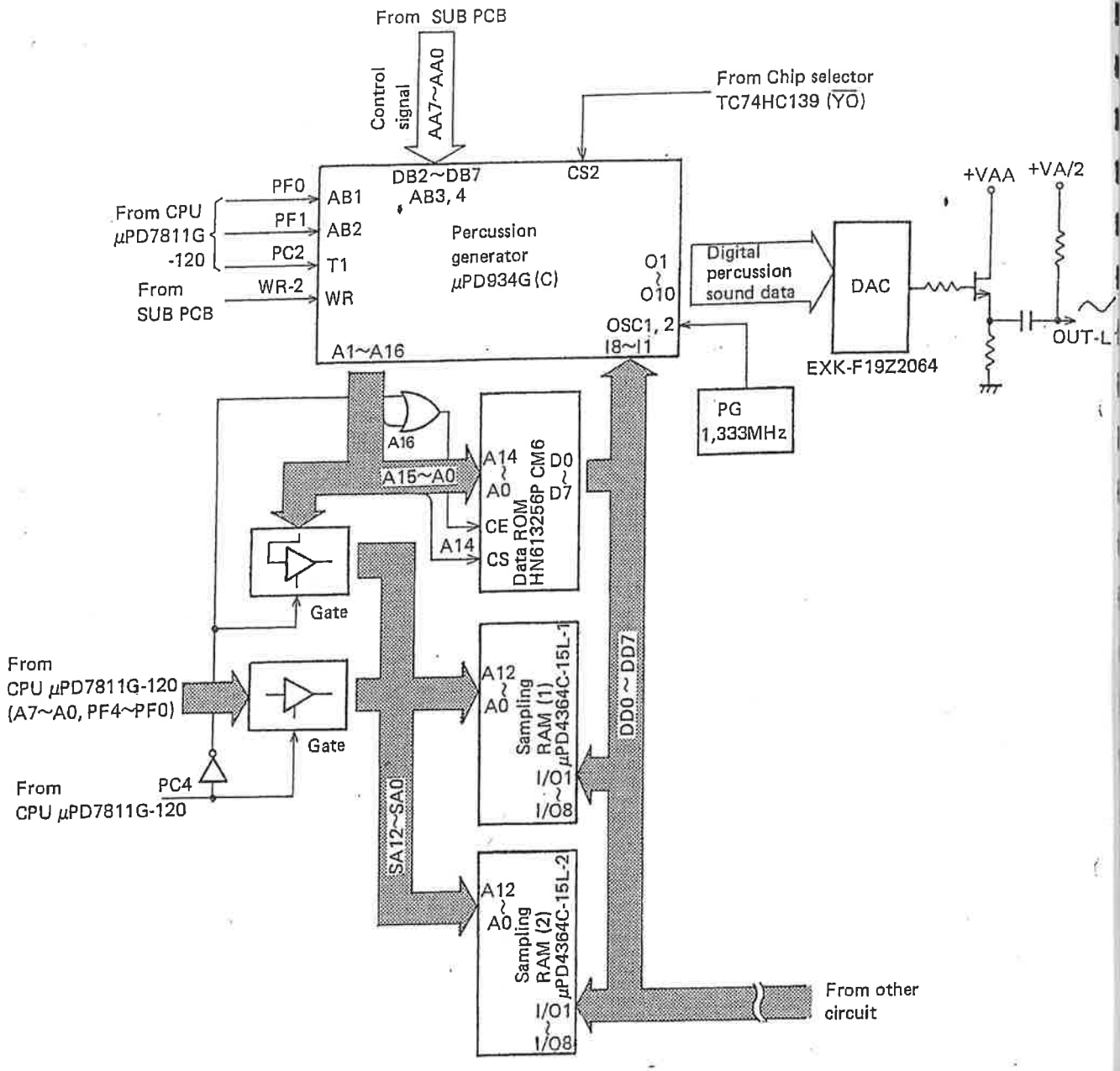


The LSI (μPD934G (B)) outputs eight kinds of digital percussion sound data received from the data ROM (HN613256P CM5).

The percussion sounds are Tom 1 ~ 3, Rim Shot, Snare Drum, Open HH, Close HH, Bass Drum.

DAC (Digital to Analog Converter) transforms the 10-bit digital signals into a stepped waveform of current. The current is converted into a voltage level by FET.

10-2. μPD934G (C Chip) Block

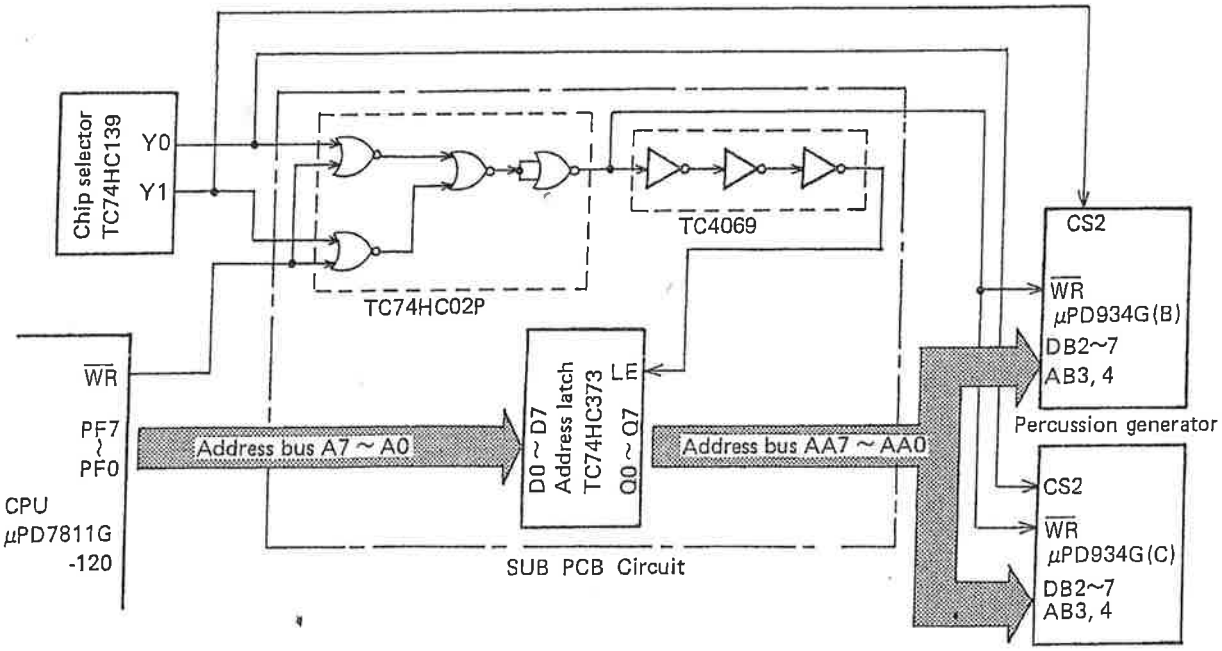


The data ROM (HN613256P CM6) contains the percussion data for Claps, Ride, Cowbell, and Crash.
The sampling RAMs (μPD4364C-15L-1, 2) store the sampling sound data for Sample 1~4.
The address signals for the sampling RAMs (μPD4364C-15L-1, 2) vary according to signal PC4 from the CPU (μPD7811G-120).
The address signals (SA12 ~ SA0) for the sampling RAM is provided from CPU (μPD7811G-120) when PC4 is "H".
The sampling RAM stores the sampling sound data.
Whereas percussion generator designates the sampling RAM's address when PC4 is "L".

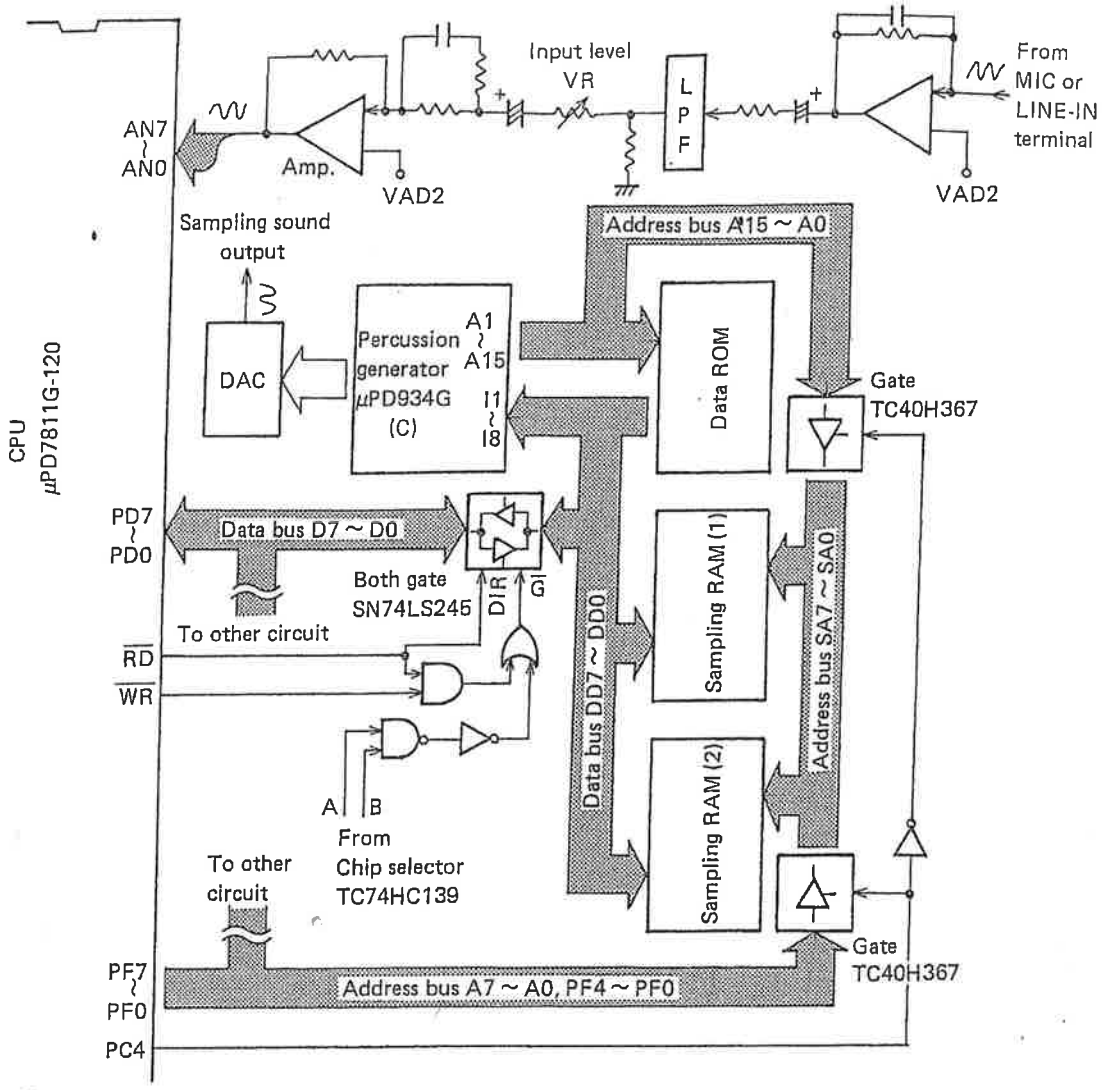
The sampling RAM outputs the sampling data to percussion generator (μPD934G(C)).
The LSI (μPD934G (C)) outputs these digital sound data received from the data ROM (HN613256 CM6) or the sampling RAM (μPD4364C-15L-1, 2).
DAC (Digital to Analog Converter) transforms the 10-bit digital signals into a stepped waveform of current. The current is converted into a voltage level by FET.

11. SUB PCB CIRCUIT

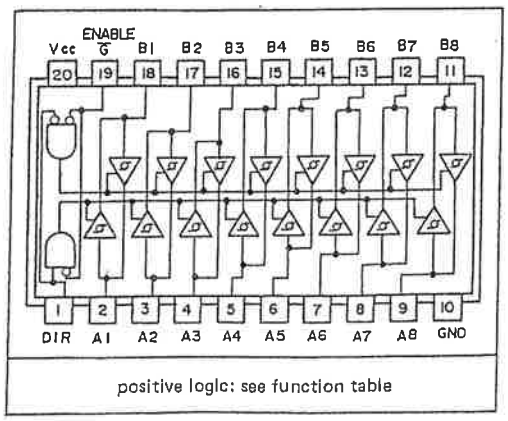
RZ-1 has a SUB PCB circuit to eliminate noise that may exist while RZ-1 is not operated.
This circuit stops the functions of percussion generators (μPD934G (B), (C)) by means of shutting the address signals in the no-operation condition.



12. SAMPLING CIRCUIT



SN74LS245 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

FUNCTION TABLE

ENABLE G	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H=high level, L=low level, X=irrelevant

(1) Process of sampling sound input

1. A sampling sound is input to terminal AN0 ~ AN7 of CPU (μPD7811G-120) from the MIC or LINE-IN terminal.
2. The input signal is converted from an analog signal to digital signals by internal DAC (Digital to Analog Convertor) in the CPU (μPD7811G-120).
3. The digital signal data are transferred to the sampling RAMs (μPD4364C-15L-1, 2), then these address signals are provided by the CPU (μPD7811G-120).

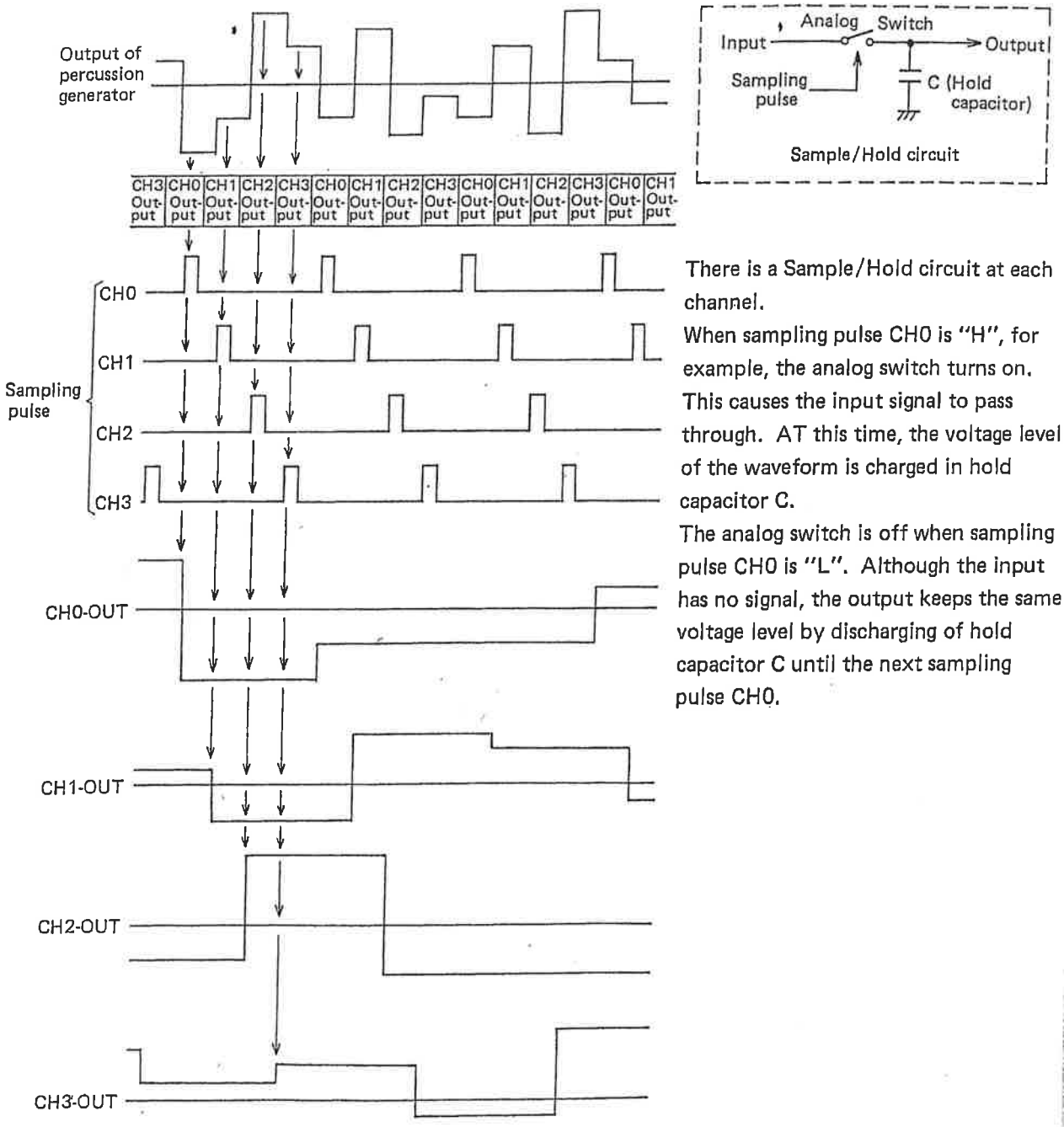
(2) Sample sound output process

1. The percussion generator (μPD934G (C)) receives the digital sampling data from the sampling RAMs. Then the address signals of the sampling RAMs (μPD4364C-15L-1, 2) are provided by the percussion generator (μPD934G (C)).
2. DAC (Digital to Analog Converter) transforms the digital sampling signal into a stepped waveform.

13. MULTIPLEXER CIRCUIT

(1) Principle

The percussion generator (μPD934G) has 4-output channels (CH0 ~ CH3), and outputs each channel with time sharing.



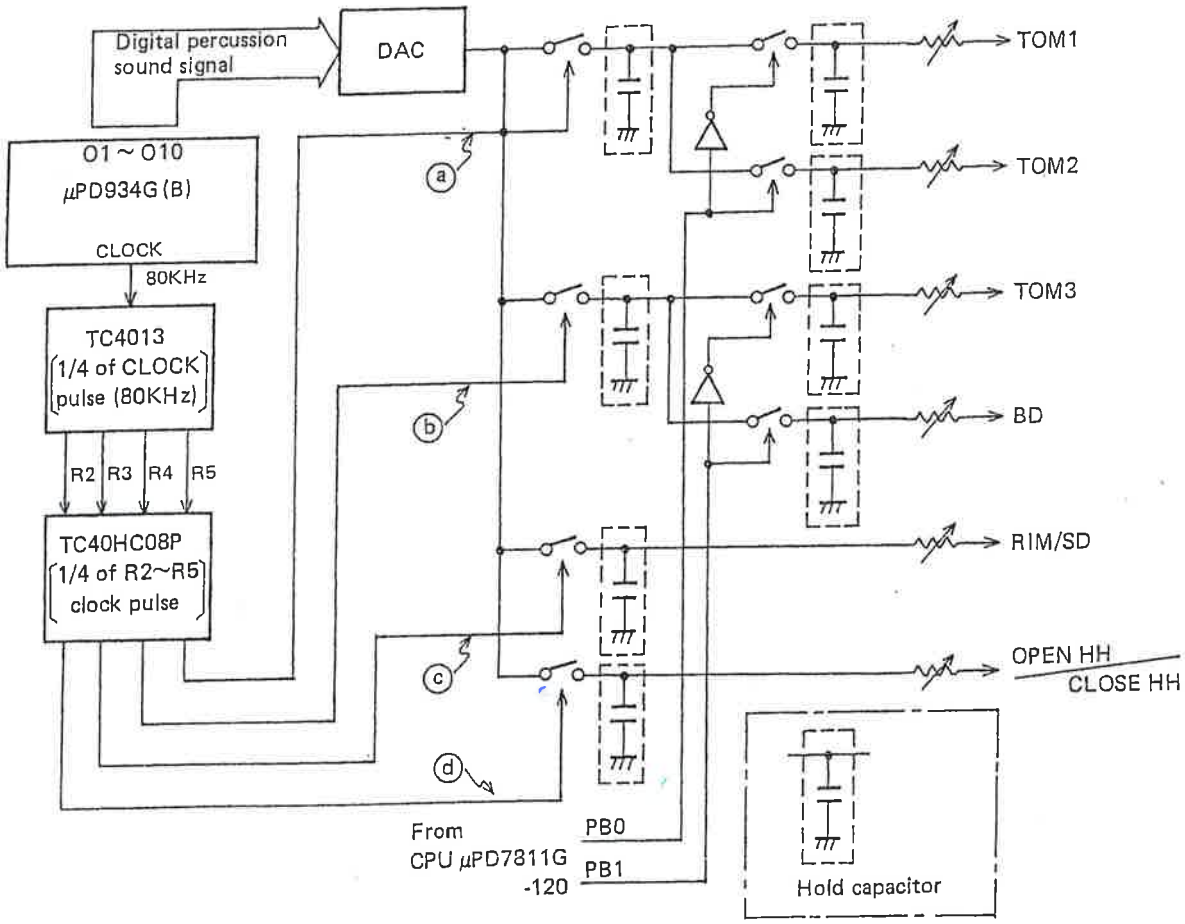
There is a Sample/Hold circuit at each channel.

When sampling pulse CH0 is "H", for example, the analog switch turns on. This causes the input signal to pass through. AT this time, the voltage level of the waveform is charged in hold capacitor C.

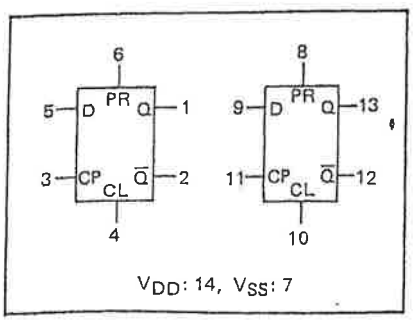
The analog switch is off when sampling pulse CH0 is "L". Although the input has no signal, the output keeps the same voltage level by discharging of hold capacitor C until the next sampling pulse CH0.

(2) Multiplexer circuit

Since the output of percussion generator (μPD934G) is time sharing, the multiplexer circuit divides the output into each percussion sound.



TC4013 BLOCK DIAGRAM



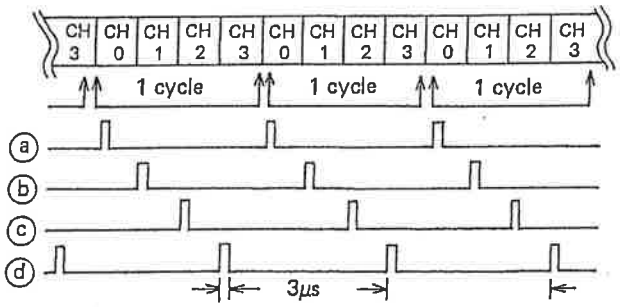
TC4013 TRUTH TABLE

INPUTS				OUTPUTS	
CL	PR	D	CP△	Q_{n+1}	$\overline{Q}_{n+1}$
L	H	*	*	H	L
H	L	*	*	L	H
H	H	*	*	L	H
L	L	L	↓	L	H
L	L	H	↓	H	L
L	L	*	↑	Q_n•	$\overline{Q}_n$•

* : Don't care
△ : Level change
• : No change

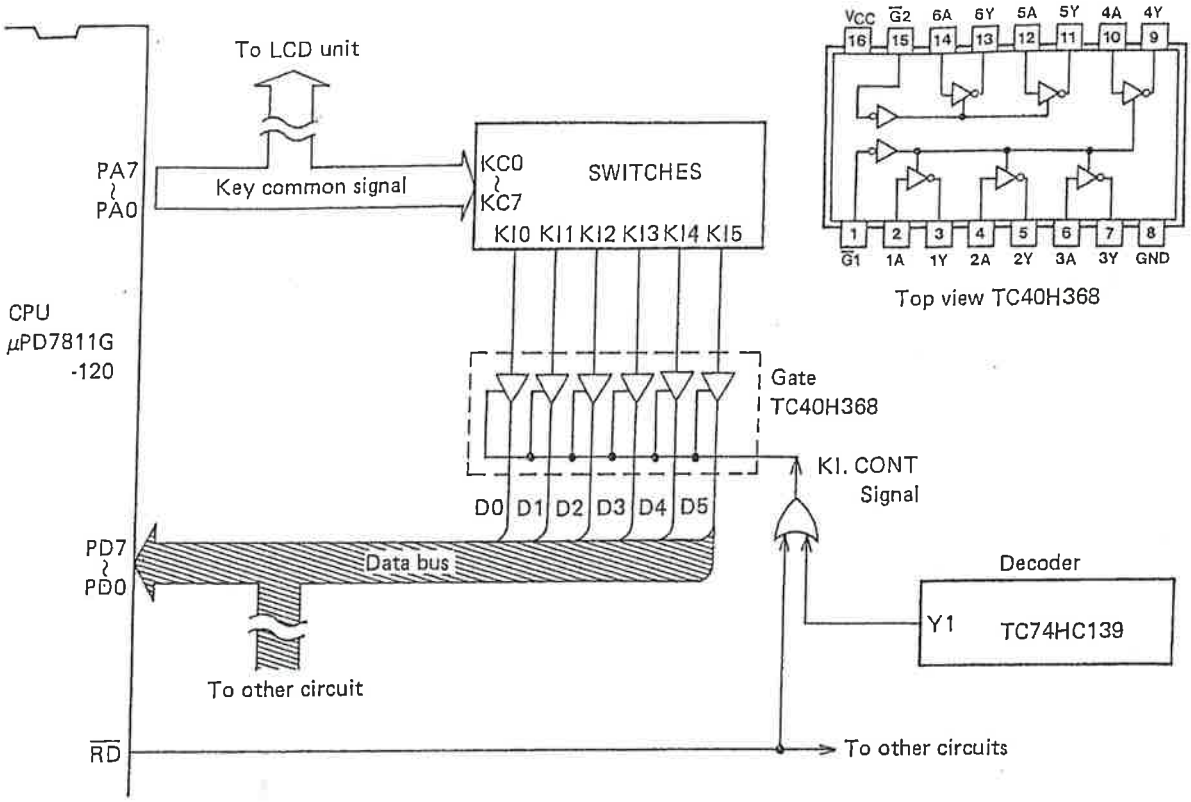
Note: This figure shows one example of a multiplexer with LSI μPD934G (B) circuit. The actual circuit differs.

As described above, the percussion generator (μPD934G) outputs the percussion sound from four channels (CH0 ~ 3) with time sharing. There are α-waveform and β-waveform at each channel. The signals PB0 and PB1 from the CPU (μPD7811G-120) divide these waveforms into two parts.



	μPD934G (B)		μPD934G (C)	
	α	β	α	β
CH0	TOM1	TOM2	CLAPS	RIDE
CH1	TOM3	BD	COWBEL	CRASH
CH2	RIM	SD	SAMPLE1	SAMPLE2
CH3	OPEN HH	CLOSE HH	SAMPLE3	SAMPLE4

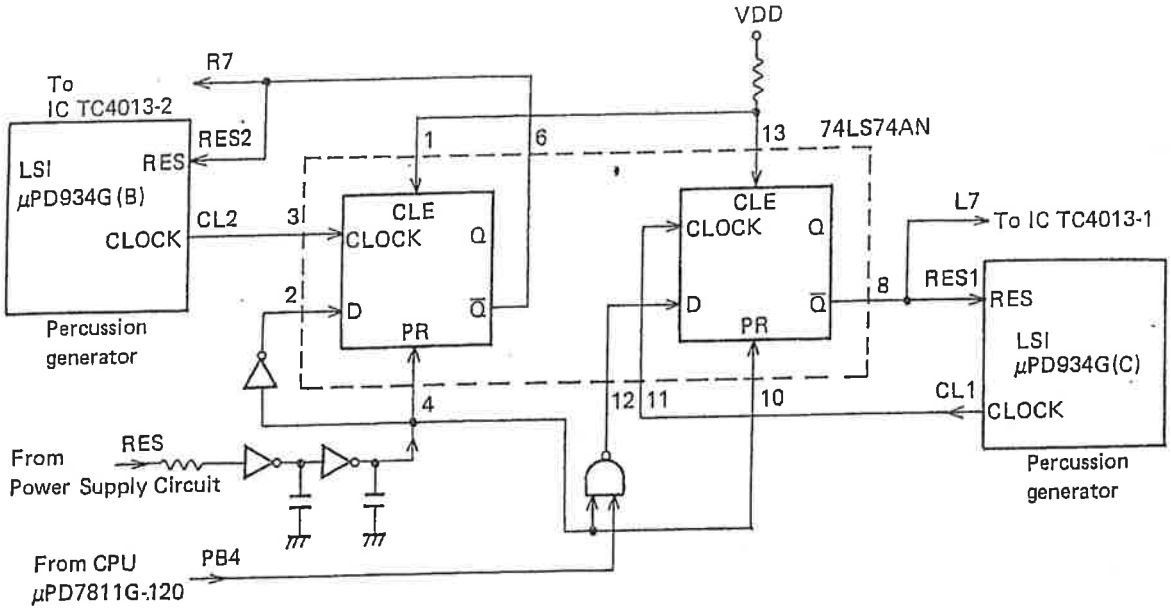
14. SWITCH MATRIX CIRCUIT



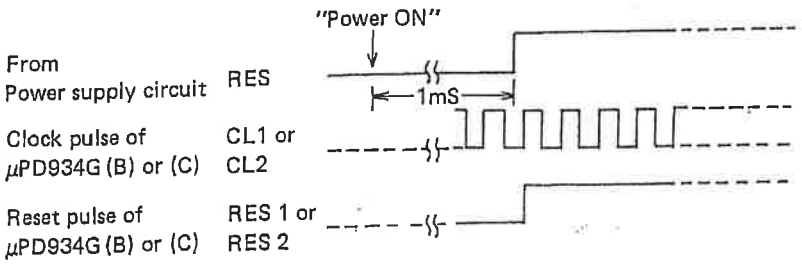
1. Key common signals (KC0 ~ KC7) are always sent to the panel switches.
2. When a switch is hit, one of the key input signals (KI0 ~ KI5) is entered into the Buffer (TC40H368).
3. Well KI. CONT signal changes to "H", a certain key input signal is entered into the data bus.
4. The following is the switch matrix table.

	KI-5	KI-4	KI-3	KI-2	KI-1	KI-0
KC0	COWBELL	CLAPS	OPEN HH	RIM	TOM3	TOM1
KC1	CRASH	RIDE	CLOSED HH	S D	B D	TOM2
KC2	ACCENT	MUTE	SAMPLE 4	SAMPLE 3	SAMPLE 2	SAMPLE 1
KC3	RESET/COPY RESET/COPY	TEMPO ▽	TEMPO △	SAMPLING	CONTINUE START	START/STOP
KC5			MIDI CLOCK	MIDI CH	MT LOAD	MT SAVE
KC6	5 (1/16)	4 (1/12)	3 (1/8)	2 (1/6)	1 (1/4)	0 (1/2)
KC7	▽ (NO)	△ (YES)	9 (1/96)	8 (1/48)	7 (1/32)	6 (1/24)

15. RESET CIRCUIT



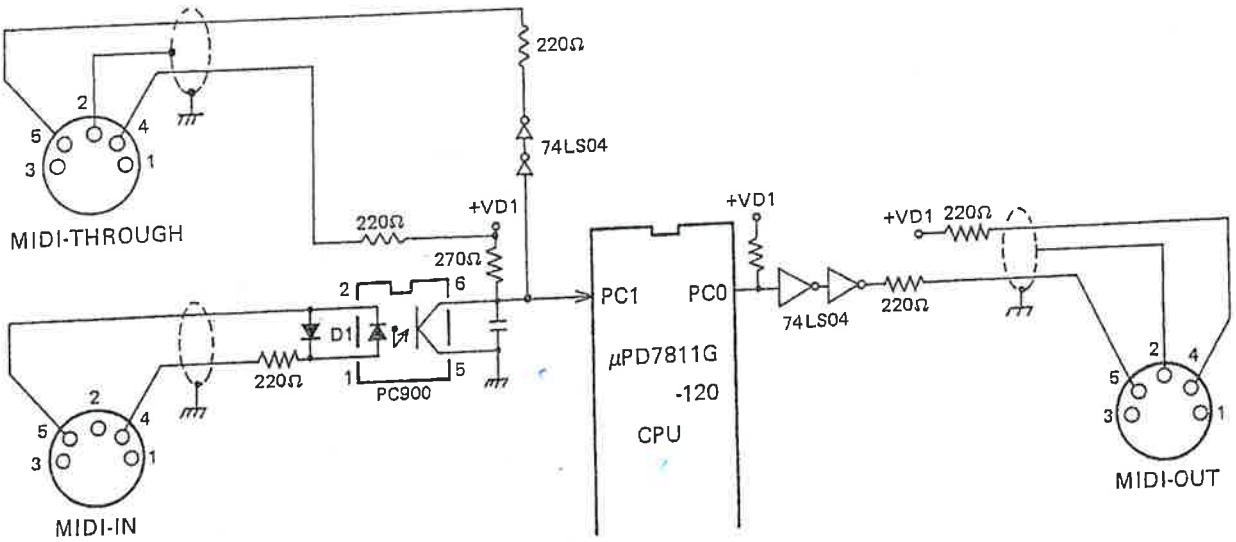
- The percussion generator (μPD934G) outputs a clock pulse to the reset circuit at Power ON (regardless of the reset pulse input).
- The percussion generator (μPD934G) is initialized by the reset pulse (RES1 or RES2). The reset pulse synchronizes with the clock pulse (CL1 or CL2) of the above.
- The percussion generator (μPD934G (C)) is initialized independently by signal PB4 of the CPU (μPD7811G-120).



16. MIDI & MT INTERFACE CIRCUITS

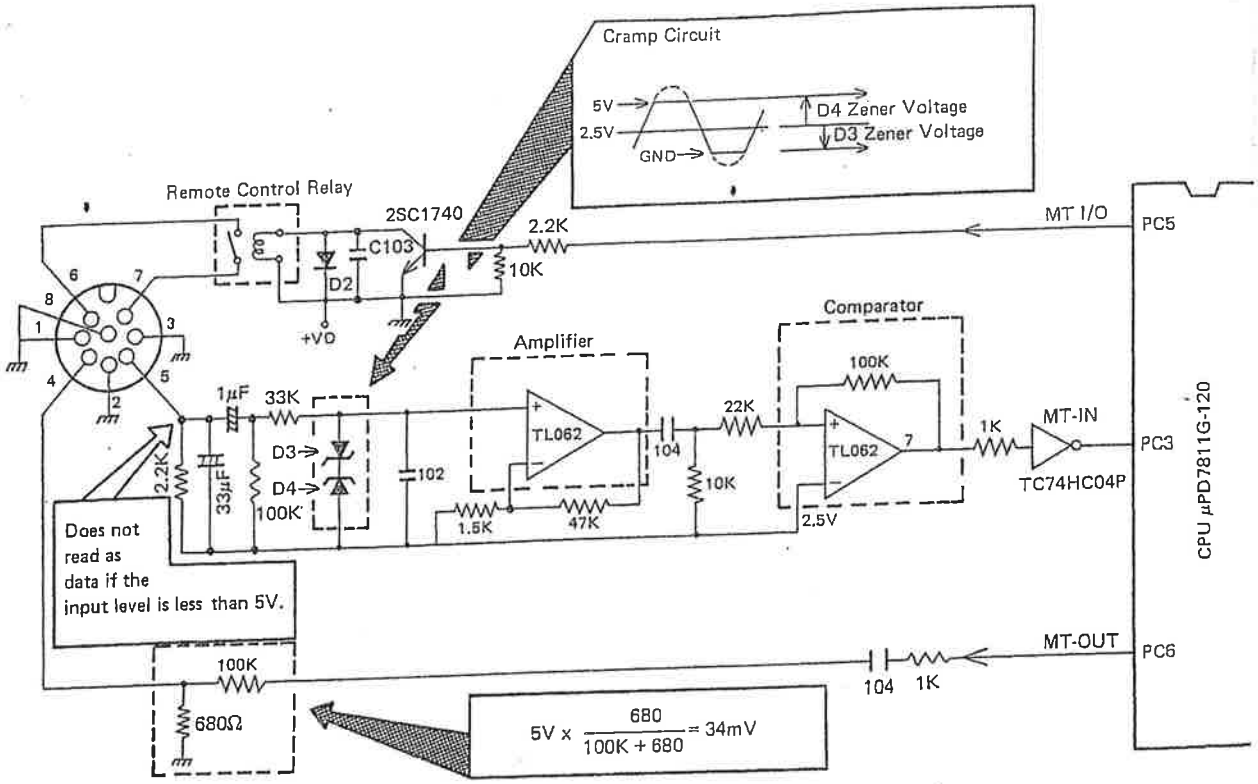
16-1. MIDI Interface Circuit

MIDI (Musical Instrument Digital Interface) is an international standard for the external control of electronic musical instruments. In other words, standardized input and output terminals are equipped in musical instruments, rhythm machines, sequencers, etc., and the music information which the machines send and receive via these terminals is made compatible by certain formatting. This standard enables a musical instrument to connect, synchronize, and sequence (memorize) to other models and even to other brands.



Serial data information from other instruments comes in from the MIDI-IN terminal and enters into CPU's PC1 terminal via photo coupler PC900. The RZ-1 is not thus electrically connected with any external instruments, which causes electric noises to be cut off.
CPU transmits MIDI data from PCO terminal.

16-2. MT Interface Circuit



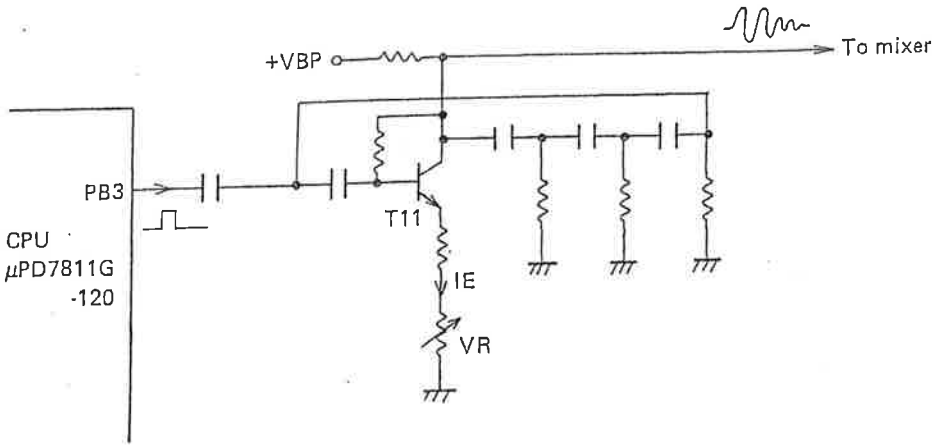
Digital data of 1 and 0 are recorded on magnetic tape as 2.4KHz and 1.2KHz sound, respectively. When data is read, a signal from a cassette tape player comes in from MT terminal pin 5. Since the voltage level varies depending on cassette tape players, the two zener diodes cramp the signal between 0 and +5 volts.

The cramped waveform is amplified by the first opamp. The second stage opamp is a comparator which examines whether the input voltage is higher or lower than 2.5V and outputs a square waveform to CPU's PC3 terminal.

As 5 volts of CPU's PC6 terminal is too high for a cassette tape recorder, it is dropped to 34 millivolts by the 100Kohm and 680ohm resistors.

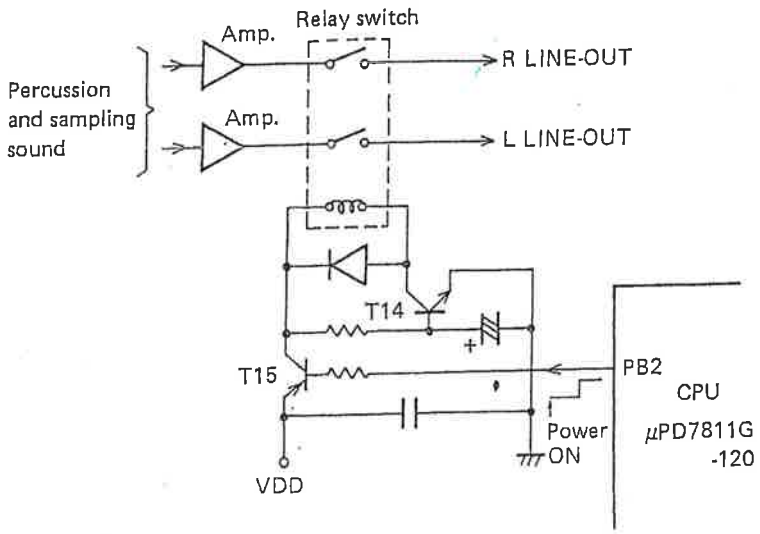
Signal PC5 from MAIN CPU turns the remote control relay on and off which controls the motor in a cassette tape player.

17. METRONOME CIRCUIT



A metronome sound is generated by CR oscillation circuits.
A trigger pulse for the oscillation comes from the CPU (μPD7811G-120). The reducing time is controlled by variable resistor VR as the emitter current IE drains to ground through it.
Emphasis and de-emphasis of the metronome sounds are controlled by the signal PB3 of the CPU (μPD7811G-120).

18. MUTE CIRCUIT AT POWER ON



The RZ-1 generates a noise from LINE-OUT terminal at Power ON. This mute circuit prevents this noise by cutting the output line.

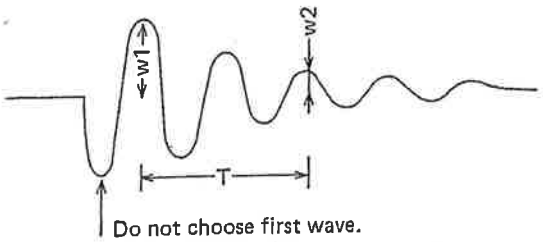
19. METRONOME SOUND ADJUSTMENT

(1) Connect an oscilloscope to the collector of T11 (refer to checkpoint Ⓐ of the PCB VIEW on page 11).

(2) Pick up wave w1 (do not choose the first wave because its voltage level is not stabilized).

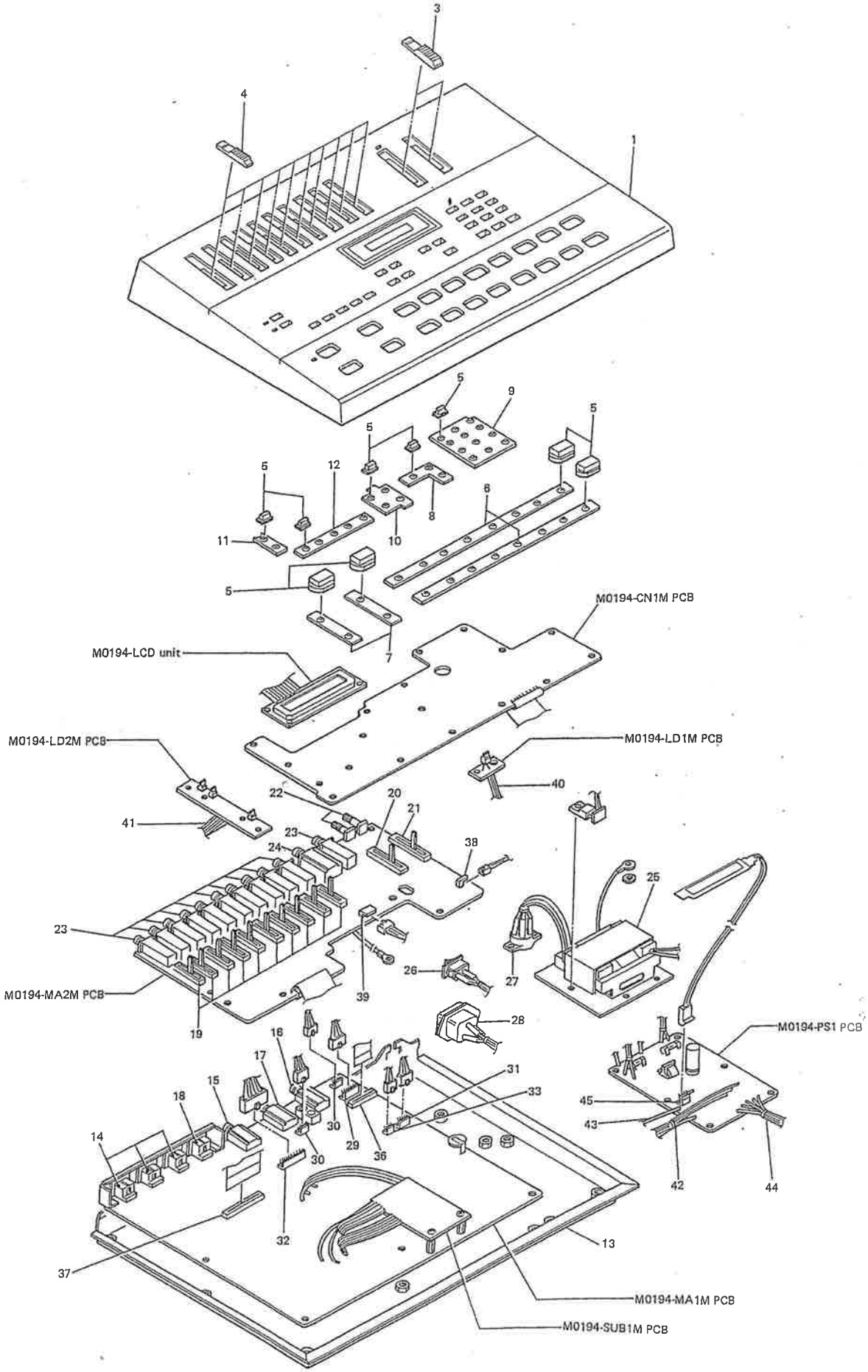
(3) Find wave w2 whose voltage level is half that of w1.

(4) Observing the oscilloscope, adjust VR so that time T between w1 and w2 is 60ms ± 10ms.



20. TROUBLESHOOTING

Trouble	Checkpoints and Possible Cause	Reference Waveform
No sound at all.	① Check voltages VDD (+5V), VA (+5V) and V9 (+12V). (faulty transistors 2SC1740, 2SA933, 2SD313, 2SC-1740 or 2SD1666 on PCB PS1M)	
	② Check clock pulse. (faulty oscillator X1, CSA1.288MK or CSA1.333MK)	WAVEFORM ①
	③ Check reset pulse. (faulty IC 74LS74, TC74HC00, or LSI μPD934G (B), (C))	WAVEFORM ②, ③
	④ Check key common signals and key input signals. (faulty IC TC40H368)	
	⑤ Check sampling pulses. (faulty IC TC40HC08 (1) ~ (3), TC4066 (1) ~ (3) on PCB MA2M, IC TC4013 (1), (2) or TC74HC04 on PCB MA1M)	
	⑥ Faulty parts (LSI μPD7811G, μPD934G (B), (C), HN4827128, HN613256P CM5, CM6, FET 2SK163M, IC μPD4364C-15L (1) ~ (3), TC74HC373, 74LS245 or TC74HC139).	
LCD does not display. (sound is OK)	Check signals PA0 ~ PA7 and PB5 ~ PB7 from CPU. (faulty LCD LM015T, PC joiner)	
Sampling impossible. (sound is OK)	Check analog sound signal at pin 33 ~ 41 of CPU. (faulty opamp MSM4558, IC TC40H367 (1) ~ (5), TC74HC08, μPD4364C-15L (1), (2))	
Distortional sound	Faulty parts (RLN EXK-F19Z2064, FET 2SK163M on PCB MA1M, opamp MSM4558 (5), FET 2SK163M1 on PCB MA2M)	WAVEFORM ④ ~ ⑪
Certain switches do not respond.	① Check the contact point of the contact rubber or poor soldering of diodes. Clean the switch PCB or re-solder the diodes on the switch PCB.	
	② Check the PC joiner contacts. Replace faulty PC joiner.	
	③ Check analog sound signals at collector of T1 ~ T10, T12, T13 on PCB MA2M. (faulty transistor T1 ~ T10, T12, T13 or opamp MSM4558 (1) ~ (4) on PCB MA2M).	


M0194-CN1M PCB
M0194-LCD unit
M0194-LD2M PCB
M0194-LD1M PCB
M0194-MA2M PCB
M0194-PS1 PCB
M0194-MA1M PCB
M0194-SUB1M PCB